CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is:

1. A method of forming a field effect transistor comprising the steps of:

selecting a substrate of single crystal semiconductor material,

forming a first sacrificial layer on said substrate,

forming a metal layer on said first sacrificial layer, said metal layer including material suitable for forming a Schottky metal-to-semiconductor barrier and having a selected work function,

forming an insulating layer over said metal layer,

forming a gate opening in said insulating layer and said metal layer,

heating said substrate, first sacrificial layer and said metal layer above a selected temperature for a time period to react said metal layer and said sacrificial layer to form a Schottky metal-to-semiconductor barrier on said substrate,

removing said sacrificial layer in said gate opening to expose said substrate,

forming a gate dielectric on said substrate in said gate opening and over the sidewalls of said opening,

forming a conductive layer on said gate dielectric in said gate opening, and

patterning said conductive layer to define a gate electrode,

said Schottky metal barrier on opposite sides of said gate electrode corresponding to the source and drain of said field effect transistor.

2. The method of claim 1 wherein said step of selecting said single crystal semiconductor material includes the step of selecting from the group consisting of GaAs, InGaAs, InP, $In_{1-x}Ga_xAs_yP_{1-y}$, Si and SiGe.

3. The method of claim 1 wherein said step of forming a first sacrificial layer includes the step of selecting from the group consisting of GaAs, InGaAs, InP, $In_{1-x}Ga_xAs_yP_{1-y}$, Si and SiGe.

4. The method of claim 1 wherein said step of forming a metal layer includes the step of selecting from the group consisting of Co, Ni, Pd, Pt, Rh, Ta, Ti and W.

5. The method of claim 1 wherein said step of forming a metal layer includes the step of forming a titanium layer and wherein said step of heating includes heating to a temperature above 700°C.

6. The method of claim 1 wherein said step of forming a metal layer includes the step of forming a platinum layer and wherein said step of heating includes heating to a temperature above 250°C.

7. The method of claim 1 wherein said step of forming a first sacrificial layer includes the step of forming a silicon germanium layer and wherein said step of heating includes heating to a temperature to form metal silicide and metal germanide to provide a Schottky barrier to the semiconductor substrate.

8. The method of claim 1 further including the step of forming source and drain contacts to said Schottky metal barrier on opposite sides of said gate electrode and wherein said step of forming a conductive layer includes forming said conductive layer

on said sidewalls of said opening.

9. A field effect transistor comprising:

a semiconductor substrate,

two spaced apart Schottky metal semiconductor compound regions forming a source and drain and defining a channel there between,

a first dielectric layer on said source and drain adjacent said channel,

a gate dielectric layer on said channel, and

a conductive layer on said gate dielectric to form a gate.

10. The field effect transistor of claim 9 wherein said metal semiconductor compound regions are selected from the group consisting of metal silicide, metal germanide, mixtures of metal silicide and metal germanide, and metal arsenide.

11. The field effect transistor of claim 9 wherein said conductive layer extends over said first dielectric layer to reduce the resistance of said gate.

12. The field effect transistor of claim 9 wherein said conductive layer extends over said first dielectric layer over a portion of the source and drain to form a T-shaped gate.

13. A method of forming a field effect transistor comprising the steps of:

selecting a substrate of single crystal semiconductor material,

forming a first layer of heavily doped semiconductor material compositionally different from said substrate to provide a different etching rate with respect to said substrate,

forming a second insulating layer,

forming an opening in said first and second layers for a gate,

forming a gate dielectric on said substrate in said opening and over the sidewalls of said opening,

forming a conductive layer on said gate dielectric in said gate opening and on said sidewalls of said opening, and

patterning said conductive layer to define a gate electrode,

said first layer on opposite sides of said gate electrode corresponding to the source and drain of said field effect transistor.

14. The method of claim 13 wherein said step of selecting said single crystal semiconductor material includes the step of selecting from the group consisting of GaAs, InGaAs, InP, $In_{1-x}Ga_xAs_yP_{1-y}$, Si and SiGe.

15. The method of claim 13 wherein said step of forming a first layer includes the step of forming a single crystal layer.

16. The method of claim 13 wherein said step of forming a first layer includes the step of forming a polycrystalline layer.

17 The method of claim 13 wherein said step of forming a first layer includes the step of selecting from the group consisting of

GaAs, InGaAs, InP, $In_{1-x}Ga_xAs_yP_{1-y}$, Si and SiGe.

18. The method of claim 13 wherein said step of forming a second layer includes the step of selecting from the group consisting of silicon dioxide and silicon nitride.

19. The method of claim 13 wherein said step of forming a conductive layer includes the step of forming over said insulating layer and wherein said step of patterning includes defining a gate electrode that extends on said sidewalls and over said insulating layer.

20. The method of claim 19 wherein said step of patterning includes defining a gate electrode that extends on said sidewalls and over said insulating layer over a portion of said source and drain to form a T-shaped gate.

21. The method of claim 13 further including the step of forming source and drain contacts to said first layer on opposite sides of said gate electrode.

22. A field effect transistor comprising:

a semiconductor substrate,

two spaced apart heavily doped semiconductor regions on said semiconductor substrate forming a source and drain and defining a channel in said substrate there between, said semiconductor regions compositionally different from said substrate to provide a selective etching rate for forming said spaced apart regions,

a first dielectric layer on said source and drain adjacent said channel,

a gate dielectric layer on said channel and on the sidewalls and adjacent said channel on said two spaced apart semiconductor regions, and

a conductive layer on said gate dielectric over said channel forming a gate.

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23. The field effect transistor of claim 22 wherein said heavily doped semiconductor regions include SiGe alloy. Composition of an alloy

24. A method of forming a field effect transistor comprising the steps of:

selecting a substrate of single crystal semiconductor material,

forming a metal layer on said substrate, said metal layer including material suitable for forming a Schottky metal-to-semiconductor barrier and having a selected work function,

forming an insulating layer over said metal layer,

forming a gate opening in said insulating layer to expose said metal layer,

heating said metal layer in said gate opening above a selected temperature for a time period in a gaseous ambient to react said metal layer and constituents in said gaseous ambient to form a gate dielectric in said gate opening on said substrate,

forming a conductive layer on said gate dielectric in said gate opening, and

patterning said conductive layer to define a gate electrode,

said Schottky metal-to-semiconductor barrier on opposite sides of said gate electrode corresponding to the source and drain of said

field effect transistor.

25. The method of claim 24 wherein said step of selecting said single crystal semiconductor material includes the step of selecting from the group consisting of silicon and silicon germanium.

26. The method of claim 24 wherein said step of forming a metal layer includes the step of selecting from the group consisting of Co, Ni, Pd, Pt, Rh, Ta, Ti and W.

27. The method of claim 24 wherein said step of forming a metal layer includes the step of forming a titanium layer and wherein said step of heating includes heating in a gaseous ambient including oxygen.

28. The method of claim 24 wherein said step of heating includes heating in a gaseous ambient selected to react with said metal of said metal layer to form a dielectric material.

29. The method of claim 1 wherein said step of heating includes heating to a temperature to form a Schottky metal semiconductor compound with the material of said substrate.

30. A field effect transistor comprising:

a semiconductor substrate,

two spaced apart metal-semiconductor compound regions forming a source and drain and defining a channel there between,

a first dielectric layer on said source and drain adjacent said channel,

a gate dielectric layer of local reacted metal of said metal used in said metal-semiconductor compound regions on said channel, and

a conductive layer on said gate dielectric to form a gate.

31. The field effect transistor of claim 30 wherein said conductive layer extends over said first dielectric layer to reduce the resistance of said gate.

32. The field effect transistor of claim 30 wherein said conductive layer extends over said first dielectric layer over a portion of the source and drain to form a T-shaped gate.

33. The field effect transistor of claim 30 wherein said gate dielectric layer includes TiO_2.

34. A method for making an FET comprising:

selecting a semiconductor substrate, having a layer of dielectric thereon,

etching a gate window in said layer of dielectric exposing said substrate,

selectively growing germanium on said substrate in said gate window wherein no germanium has grown on said layer of dielectric,

using the germanium as a mask, implanting shallow regions of dopant ions to form the source and drain,

removing said germaniun,

forming a gate oxide in said gate window,

forming a layer of conductive material on said gate oxide and on said layer of dielectric, and

patterning said layer of conductive material to form a gate.

35. A method for making an FET comprising:

selecting a semiconductor substrate, having a layer of dielectric thereon,

etching a gate window in said layer of dielectric exposing said substrate,

forming a layer of resist on said layer of dielectric and on said exposed substrate in said gate window, exposing and developing said resist to remove resist from said gate window to expose said substrate,

forming a blanket layer of titanium over said resist and on said exposed substrate in said gate window,

removing the remainder of said resist and titanium on said resist,

using the titanium as a mask, implanting shallow regions of dopant ions to form the source and drain,

removing said titanium,

forming a gate oxide in said gate window,

forming a layer of conductive material on said gate oxide and on said layer of dielectric, and

patterning said layer of conductive material to form a gate.

36. The method of claim 13 further including the step of forming an epitaxial layer of second semiconductor material on said substrate in said opening to provide a raised channel above said substrate prior to said step of forming a gate dielectric.

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